In the Claims:

Please amend the claims as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A hybrid MOS-bipolar device comprising a trench MOS device having at least source, gate, drain and body regions, the gate and ~~base~~ the body being shorted together and biased positively relative to the drain.

2. (Currently Amended) The hybrid MOS-bipolar device of claim l ~~wherein said~~ further comprising a gate oxide having ~~has~~ a single oxide thickness of under 600A.

3. (Currently Amended) The hybrid MOS-bipolar device of claim 1 ~~wherein said~~ further comprising a gate oxide having ~~has a~~ multiple oxide thicknesses for formation of gate and field-oxide regions.

4. (Original) The hybrid MOS-bipolar device of claim 2 having a square trench geometry.

5. (Original) The hybrid MOS-bipolar device of claim 2 having a circular geometry.

6. (Currently Amended) A method of implementing a hybrid MOS-bipolar device that includes a trench MOS device having a source, a body and a gate, comprising shorting together the body and the gate ~~of a trench MOS device~~ and positively biasing ~~the~~ an electrode connected to the shorted body and gate.

7. (Currently Amended) The method of claim 6 wherein the trench MOS device includes a gate oxide having a thickness that varies along the length thereof.

8. (Original) The method of claim 7 wherein the gate oxide thickness varies by having two substantially discrete levels of thickness.

9. (Currently Amended) The method of claim 8 wherein said hybrid MOS-bipolar device has a PI region and an Ndrift region, and wherein the gate oxide has a first gate oxide thickness ~~is fabricated~~ adjacent said PI region and a second and thicker gate oxide thickness ~~is fabricated~~ adjacent said Ndrift region.

10. (Currently Amended) A hybrid MOS-bipolar device comprising a PI region, an Ndrift region, a body, a gate, a drain and a source, said device being configured with its body ~~base~~ and gate shorted together, said device including ~~having~~ a gate oxide having a thickness of a first value adjacent said PI region[[,]] and having a ~~gate oxide~~ thickness of a second value adjacent said Ndrift region.

11. (Original) The hybrid MOS bipolar device of claim 10, wherein said gate and said body are positively biased.

12. (Currently Amended) A method of making a hybrid MOS-bipolar device comprising doping a PI region to optimize said region for said MOS device, and fabricating a gate electrode ~~from~~ to optimize a bipolar component of said hybrid MOS-bipolar device.

13. (Currently Amended) The method of claim 12 further comprising making a gate oxide having a thickness that varies along the length thereof.

14. (Currently Amended) The method of claim 13 wherein said gate oxide thickness is greater in a region adjacent said PI region than it is in a region adjacent said Ndrift region.

15. (Original) The method of claim 14 wherein said device is constructed using a double metal process flow.

16. (Currently Amended) A hybrid bipolar-MOS device ~~having~~ comprising a first region serving as a source and an emitter, a second region serving as a body and a base, and a third region serving as a gate ~~and base~~, the gate and the body ~~base~~ being shorted together and positively biased.

17. (Currently Amended) The hybrid bipolar-MOS device of claim 16 ~~having~~ further comprising a fourth region that serves as both a drain and a collector.

18. (Currently Amended) The hybrid bipolar-MOS device of claim 17 ~~having~~ wherein the device has a breakdown voltage of approximately 200 volts.

19. (Currently Amended) The hybrid bipolar-MOS device of claim 17 further comprising a gate oxide having a single ~~gate oxide~~ thickness of approximately 380-600 Angstroms ~~Angstoms~~.

20. (Currently Amended) The hybrid bipolar-MOS device of claim 17 further comprising a gate oxide having ~~plural gate oxide~~ a plurality of thicknesses.

21. (Original) The hybrid MOS-bipolar device of claim 2 having a stripe geometry.

22. (New) A hybrid MOS-bipolar device comprising:

a MOS device having a trench gate, a source, a drain and a body, the trench gate and the body being shorted together and biased positively relative to the drain;

a bipolar device having an emitter, a collector, a base and a gate formed by the trench gate, the emitter and the source being formed by a common region, the base and the body

being formed by a common region, and the collector and the drain being formed by a common region;

a substrate that includes a PI region and an N drift region, the trench gate extending from a top surface of the substrate through the PI region into the N drift region;

a first electrode coupled to the trench gate, the body and the base; and

a second electrode coupled to the source and the emitter.

23. (New) The device of claim 22, further comprising a gate oxide that insulates the trench gate from the substrate, the gate oxide having a first thickness in a region adjacent the N drift region and having a second thickness adjacent the PI regions, the first thickness being greater than the second thickness.

24. (New) The device of claim 22, further comprising a third electrode coupled to the drain and collector, the third electrode located on a bottom surface of the substrate.